What is claimed is:

1. A method of fabricating a polysilicon line, comprising:

forming a patterned hard mask layer over a polysilicon layer;

patterning the polysilicon layer to provide a hard mask-capped polysilicon line having a first width; and

isotropically removing portions of said polysilicon line to a second width.

2. The method of claim 1, wherein said second width is sub-minimum groundrule.

3. The method of claim 1, further including removing said patterned hard mask layer

4. The method of claim 1, wherein said patterned hard mask layer comprises silicon oxide.

5. The method of claim 1, wherein isotropically removing portions of said polysilicon line comprises converting a

surface layer of said polysilicon line to an oxide layer and isotropically etching said oxide layer.

6. The method of claim 1, wherein the step of removing portions of the polysilicon line comprises a treatment in a saturated aqueous solution of O_3 followed by etching in a solution comprising 1 part 49% HF in 50 to 300 parts of water.

7. The method of claim 1, wherein the step of removing portions of the polysilicon line comprises a treatment in a saturated aqueous solution of O_3 followed by etching in an HF containing vapor.

8. The method of claim 1, wherein the step of removing portions of the polysilicon line comprises etching in a solution of 1 part 49% HF, 100 to 200 parts 69% HNO_3 and 100 to 200 parts 85% H_3PO_4.

9. The method of claim 1, wherein the step of removing portions of the polysilicon line comprises etching in a

solution of 1.3 parts 30% NH_4OH, 3.1 parts 31% H_2O_2 and 80 to 100 parts of water.

10. A method of reducing transistor gate dimensions, comprising:

forming a patterned hard mask layer over a polysilicon layer, said polysilicon layer formed over a gate dielectric layer;

patterning the polysilicon to provide a hard mask-capped polysilicon electrode having a first width; and

isotropically removing portions of the polysilicon electrode to a second width.

11. The method of claim 10, wherein said second width is sub-minimum groundrule.

12. The method of claim 10, further including removing said patterned hard mask layer.

13. The method of claim 10, wherein said patterned hard mask layer comprises silicon oxide.

14. The method of claim 10, wherein isotropically removing portions of said polysilicon electrode comprises converting

a surface layer of said polysilicon line to an oxide layer and isotropically etching said oxide layer.

15. The method of claim 10, wherein the step of removing portions of the polysilicon electrode comprises a treatment in a saturated aqueous solution of O_3 followed by etching in a solution comprising 1 part 49% HF in 50 to 300 parts of water.

16. The method of claim 10, wherein the step of removing portions of the polysilicon electrode comprises a treatment in a saturated aqueous solution of O_3 followed by etching in an HF containing vapor.

17. The method of claim 10, wherein the step of removing portions of the polysilicon electrode comprises etching in a solution of 1 part 49% HF, 100 to 200 parts 69% HNO_3 and 100 to 200 parts of 85% H_3PO_4.

18. The method of claim 10, wherein the step of removing portions of the polysilicon electrode comprises etching in a

solution of 1.3 parts 30% NH_4OH, 3.1 parts 31% H_2O_2 and 80 to 100 parts of water.

19. A method of forming a transistor gate, comprising:

forming a dielectric layer on a top surface of a substrate;

forming a polysilicon layer on a top surface of said dielectric layer;

forming a patterned hard mask layer on a top surface of said polysilicon layer;

patterning the polysilicon to provide a hard mask-capped polysilicon electrode having a first width; and

isotropically removing portions of the polysilicon electrode to a second width.

20. The method of claim 19, wherein said second width is sub-minimum groundrule.

21. The method of claim 19, further including removing said patterned hard mask layer.

22. The method of claim 19, further including simultaneously removing portions of said dielectric layer not covered by said polysilicon gate electrode and said patterned hard mask.

23.The method of claim 19, wherein said hard mask layer and said dielectric layer comprise silicon oxide.

24. The method of claim 19, wherein said substrate is selected from the group consisting of silicon, silicon on insulator, gallium arsenide and sapphire.

25. The method of claim 19, wherein the step of removing portions of the polysilicon electrode comprises a treatment in a saturated aqueous solution of O_3 followed by etching in a solution comprising 1 part 49% HF in 50 to 300 parts of water.

26. The method of claim 19, wherein the step of removing portions of the polysilicon electrode comprises a treatment in a saturated aqueous solution of O_3 followed by etching in an HF containing vapor.

27. The method of claim 19, wherein the step of removing portions of the polysilicon electrode comprises etching in a solution of 1 part 49% HF, 100 to 200 part 69% HNO_3 and 100 to 200 parts of H_3PO_4.

28. The method of claim 19, wherein the step of removing portions of the polysilicon electrode comprises etching in a solution of 1.3 parts 30% NH_4OH, 3.1 parts 31% H_2O_2 and 80 to 100 parts of water.

29. A method of forming a transistor gate, comprising:

forming a dielectric layer on a top surface of a substrate;

forming a polysilicon layer on a top surface of said dielectric layer;

forming a patterned hard mask layer on a top surface of said polysilicon layer;

patterning the polysilicon to provide a hard mask-capped polysilicon electrode having a first width;

measuring said first width;

comparing said first width to a target width and determining a delta;

calculating an etch time or a number of polysilicon oxidation/isotropic polysilicon etch cycles based on said delta; and

performing an isotropic polysilicon etch for the calculated time or performing the calculated number of polysilicon oxidation/isotropic polysilicon etch cycles.

30. The method of claim 29, wherein said target width is sub-minimum groundrule.

31. The method of claim 29, further including removing said patterned hard mask layer.

32. The method of claim 29, further including simultaneously removing portions of said dielectric layer not covered by said polysilicon gate electrode and said patterned hard mask.

33.The method of claim 29, wherein said hard mask layer and said dielectric layer comprise silicon oxide.

34. The method of claim 29, wherein said substrate is selected from the group consisting of silicon, silicon on insulator, gallium arsenide and sapphire.

35. A polysilicon line fabricated by the process comprising:

forming a patterned hard mask layer over a polysilicon layer;

patterning the polysilicon to provide a hard mask-capped polysilicon line having a first width; and

isotropically removing portions of said polysilicon line to a second width.

36. The polysilicon line of claim 35, wherein said second width is sub-minimum groundrule.

37. The polysilicon line of claim 35, wherein said substrate is selected from the group consisting of silicon, silicon on insulator, gallium arsenide and sapphire.

38. A polysilicon transistor gate fabricated by the process comprising:

forming a patterned hard mask layer over a polysilicon layer, said polysilicon layer formed over a gate dielectric layer;

patterning the polysilicon to provide a hard mask-capped polysilicon electrode having a first width;

isotropically removing portions of said polysilicon electrode to a second width; and

removing said patterned hard mask layer.

39. The polysilicon transistor gate of claim 38, wherein said second width is sub-minimum groundrule.

40. The polysilicon transistor gate of claim 39, wherein said substrate is selected from the group consisting of silicon, silicon on insulator, gallium arsenide and sapphire.

41. A polysilicon transistor gate fabricated by the process comprising:

forming a dielectric layer on a top surface of a substrate;

forming a polysilicon layer on a top surface of said dielectric layer;

forming a patterned hard mask layer on a top surface of said polysilicon layer;

patterning the polysilicon to provide a hard mask-capped polysilicon electrode having a first width;

isotropically removing portions of said polysilicon electrode to a second width; and

removing said patterned hard mask layer.

42. The polysilicon transistor gate of claim 41, wherein said second width is sub-minimum groundrule.

43. The polysilicon transistor gate of claim 41, wherein said substrate is selected from the group consisting of silicon, silicon on insulator, gallium arsenide and sapphire.